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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
09/852,220	05/09/2001	Shunpei Yamazaki	SEL 259	4950

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EXAMINER	
ABDULSELAM, ABBAS I	
ART UNIT	**PAPER NUMBER**
2677	

DATE MAILED: 02/07/2006

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	09/852,220	YAMAZAKI ET AL.	
	Examiner	Art Unit	
	Abbas I. Abdulselam	2677	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) OR THIRTY (30) DAYS, WHICHEVER IS LONGER, FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on 10/31/05.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) 1-3,6-10,12-21,23-25,27-29,31-33,35-37,40,41,43 and 45-60 is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☐ Claim(s) _____ is/are allowed.

6)☒ Claim(s) 1-3,6-10,12-21,23-25,27-29,31-33,35-37,40,41,43 and 45-60 is/are rejected.

7)☐ Claim(s) _____ is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☐ The drawing(s) filed on _____ is/are: a)☐ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☒ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☒ All b)☐ Some * c)☐ None of:

1.☒ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date 10/31/05.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Continued Examination Under 37 CFR 1.114

1. A request for continued examination under 37 CFR 1.114, including the fee set forth in 37 CFR 1.17(e), was filed in this application after final rejection. Since this application is eligible for continued examination under 37 CFR 1.114, and the fee set forth in 37 CFR 1.17(e) has been timely paid, the finality of the previous Office action has been withdrawn pursuant to 37 CFR 1.114. Applicant's submission filed on 10/31/05 has been entered.

Response to Arguments

2. With respect to claims 1-4, 6-10, 12-18 and 52-53, applicant's arguments filed on 10/31/05 have been fully considered but they are not persuasive.

With respect to claims 19-21, 23-25, 27-29, 31-33, 35-37, 40-41, 43, 45-51 and 55-60, Applicant's arguments have been considered but are moot in view of the new ground(s) of rejection.

Applicant argues that the cited references alone or in combination do not teach, "all semiconductor elements in the display portion and the driver circuit are n-channel type semiconductor elements".

However, as shown in the art rejection below, Shinotsuka reaches an MOS image sensor 1 is comprised of a multiplicity of pixels (photosensors) 4 arranged in a rectangular array or matrix, a row driver circuit 2 for selectively driving pixels in each row of the pixel array, and a column driver circuit 3 for selectively driving pixels 4 in each column of the pixel array.

Shinotsuka discloses as shown in Fig. 2 a circuit diagram of one of the pixels (photosesnors) of the MOS image sensor in which the transistors used are n-channel MOS transistors (col. 4, lines 41-50).

It would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Masuda's liquid crystal display system shown in Fig. 2 to adapt Shinotsuka's use of n-channel MOS transistors as demonstrated in Fig. 2 because the use of n-channel MOS transistors helps detect and display an image on a display device as taught by Shinotsuka (col. 5, lines 58-61).

Applicant argues that the cited references alone or in combination do not teach "a display portion comprising a current control element and the driver circuit comprising an inverter circuit". However, as shown in the art rejection below, Masuda teaches an arrangement of a scanning line drive circuit (201a), and discloses that the scanning circuit section includes a select control circuit section for generating an n-bit input numeral signal (n: 2 or more positive integer) and an inverted replica of the input numeral (col. 2, lines 65-67). Furthermore, Shinotsuka teaches as illustrated in Fig. 2 a transistor Q2 performing voltage-to-current conversion so that the detection voltage VDO can be taken out from the photo sensor 4ij in the form of a sensor current signal. Shinotsuka discloses that by the switching an operation of the transistor Q3, the sensor current signal generated by the transistor Q2 is selectively supplied to the external circuit (col. 4, lines 62-67 and col. 5, lines 1-8). Therefore, Masuda in view of Shinotsuka reads over the argued limitation

In response to applicant's argument that there is no suggestion to combine the references, the examiner recognizes that obviousness can only be established by combining or modifying the teachings of the prior art to produce the claimed invention where there is some teaching, suggestion, or motivation to do so found either in the references themselves or in the knowledge generally available to one of ordinary skill in the art. See *In re Fine*, 837 F.2d 1071, 5 USPQ2d 1596 (Fed. Cir. 1988)and *In re Jones*, 958 F.2d 347, 21 USPQ2d 1941 (Fed. Cir. 1992). In this case, both Masuda et al and Shinotsuka et al teach about display devices and one of ordinary skill in the art would have looked toward Shinotsuka for the manner by which display elements are configured.

. *Claim Rejections - 35 USC § 103*

3. The following is a quotation of 35 U.S.C. 103(a) which forms the basis for all obviousness rejections set forth in this Office action:

> (a) A patent may not be obtained though the invention is not identically disclosed or described as set forth in section 102 of this title, if the differences between the subject matter sought to be patented and the prior art are such that the subject matter as a whole would have been obvious at the time the invention was made to a person having ordinary skill in the art to which said subject matter pertains. Patentability shall not be negatived by the manner in which the invention was made.

Claims 1-4, 6-10, 12-18 and 52-53 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda et al. (USPN 6107983) in view Shinotsuka et al. (USPN 6191408).

Regarding claim 1, 7 and 13, Masuda teaches a liquid crystal display device (101) with a substrate (111), which includes driver circuits (210a, 201b, 301a, 301b), and a plurality of thin

film transistors, TFTs (165) coupled with pixel electrodes (col. 5, lines 28-46 and Fig. 2 (210a, 201b, 301a, 301b)). Masuda also teaches that the driving circuit (201a) includes a logic circuit section (215a), which in turn includes two 2-input NAND gates NA1 and NA2 (col. 6, lines 34-45 and Fig. 3 (NAND)). Furthermore, Masuda points out the use of a decoder having a plurality of logic circuits (col. 1, lines 60-67 and col. 2, lines 1-5). Masuda teaches the use of various types of liquid crystal display device including a display device with an element of light modulation, and a display element with variable light emitting capabilities (col. 15, lines 32-4). However, Masuda does not teach all semiconductor elements being n-channel type semiconductor elements. Shinotsuka on the other hand discloses a semiconductor fabrication process in which type of transistors used are n-channel MOS transistors (Q1, Q2) (Fig. 2 (Q1, Q2) and col. 4, lines 41-50).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Masuda's liquid crystal display system shown in Fig. 2 to adapt Shinotsuka's use of n-channel MOS transistors as demonstrated in Fig. 2 because the use of n-channel MOS transistors helps detect and display an image on a display device as taught by Shinotsuka (col. 5, lines 58-61).

Regarding claims 4, 10 and 14, Shinotsuka's teaches a circuit diagram of a pixel (Fig. 2 (Q1, Q2) and col. 4, lines 41-50).

Regarding claims 2, 8 and 15, Masuda teaches the use of a substrate (Fig. 2 (111) and col. 5, lines 28-46).

Regarding claims 3, 9 and 16, Masuda teaches the use of TFT (165) (Fig. 2 (165) and col. 30-46).

Regarding claims 6, 12, and 17-18, Masuda teaches the use of the liquid crystal projector 1 with three liquid crystal display devices 101, 501 and 601 (col. 4, lines 1-67 and col. 5, lines 1-13).

Regarding claims 52-54, Shinotsuka reaches an MOS image sensor 1 is comprised of a multiplicity of pixels (photosensors) 4 arranged in a rectangular array or matrix, a row driver circuit 2 for selectively driving pixels in each row of the pixel array, and a column driver circuit 3 for selectively driving pixels 4 in each column of the pixel array. Shinotsuka discloses as shown in Fig. 2 a circuit diagram of one of the pixels (photosesnors) of the MOS image sensor in which the transistors used are n-channel MOS transistors (col. 4, lines 41-50).

4. Claims 19-21, 23-25, 27-29, 31-33, 35-37, 40-41, 43, 45-51 and 55-60 are rejected under 35 U.S.C. 103(a) as being unpatentable over Masuda et al. in view of Shinotsuka et al. and Tsutsumi et al. (USPN 6713748)

Regarding claims 19, 24, 28, 32, 36 and 41, Masuda teaches a liquid crystal display device (101) with a substrate (111), which includes driver circuits (210a, 201b, 301a, 301b), and a plurality of thin film transistors, TFTs (165) coupled with pixel electrodes (col. 5, lines 28-46 and Fig. 2 (210a, 201b, 301a, 301b)). Masuda also teaches that the driving circuit (201a) includes a logic circuit section (215a), which in turn includes two 2-input NAND gates NA1 and NA2 (col. 6, lines 34-45 and Fig. 3 (NAND)). Furthermore, Masuda points out the use of a decoder having a plurality of logic circuits (col. 1, lines 60-67 and col. 2, lines 1-5). Masuda teaches the

use of various types of liquid crystal display device including a display device with an element of light modulation, and a display element with variable light emitting capabilities (col. 15, lines 32-4). In addition, Masuda teaches either one of the scanning line drive circuits 201a, 201b and video signal line drive circuits 301a, 301b or, one of sets of drive circuits 201a, 201b and 301a, 301b is constructed of a plurality of stages of shift registers (col. 5, lines 28-46).

However, Masuda does not teach all semiconductor elements being n-channel type semiconductor elements. Shinotsuka on the other hand discloses a semiconductor fabrication process in which type of transistors used are n-channel MOS transistors (Q1, Q2) (Fig. 2 (Q1, Q2) and col. 4, lines 41-50).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Masuda's liquid crystal display system shown in Fig. 2 to adapt Shinotsuka's use of n-channel MOS transistors as demonstrated in Fig. 2 because the use of n-channel MOS transistors helps detect and display an image on a display device as taught by Shinotsuka (col. 5, lines 58-61).

Masuda does not teach first and second semiconductor elements such that a gate of the second semiconductor element is connected to a drain of the first semiconductor element.

Tsutsumi on the other hand discloses as shown in Fig. 8B a circuit in which the gates are connected to the drains of the respective TFTs Tr1 to Trx (col. 10, lines 63-67).

Therefore, it would have been obvious to one of ordinary skill in the art at the time the invention was made to modify Masuda's liquid crystal display system shown in Fig. 2 to incorporate Tsutsumi's arrangement of transistors as illustrated in Fig. 8B because the use of

transistors helps form planar arrangement of pixels in an image detection device as taught by Tsutsumi.

Regarding claims 20, 25, 29, 33, 37and 43, Masuda teaches a pair of electrode substrates111 and 191 (col. 5, lines 19-26).

Regarding claim 21, Masuda teaches the use of TFT (165) (Fig. 2 (165) and col. 30-46).

Regarding claims 23, 27, 31, 35, 40 and 45, Masuda teaches the use of the liquid crystal projector 1 with three liquid crystal display devices 101, 501 and 601 (col. 14, lines 5-20).

Regarding claims 46-51, Shinotsuka's teaches a circuit diagram of a pixel (Fig. 2 (Q1, Q2) and col. 4, lines 41-50).

Regarding claims 55-60, Shinotsuka reaches an MOS image sensor 1 is comprised of a multiplicity of pixels (photosensors) 4 arranged in a rectangular array or matrix, a row driver circuit 2 for selectively driving pixels in each row of the pixel array, and a column driver circuit 3 for selectively driving pixels 4 in each column of the pixel array. Shinotsuka discloses as shown in Fig. 2 a circuit diagram of one of the pixels (photosesnors) of the MOS image sensor in which the transistors used are n-channel MOS transistors (col. 4, lines 41-50).

5. Any inquiry concerning this communication or earlier communications from the examiner should be directed to Abbas I. Abdulselam whose telephone number is (571) 272-7685. The examiner can normally be reached on Monday through Friday from 9:00 A.M. to 5:30 P.M.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Amr Awad can be reached on (571) 272-7764. The fax phone number for the organization where this application or proceeding is assigned is (571) 273-8300.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

Abbas abdulselam

Examiner

Art Unit 2677

January 31, 2006

AMR A. AWAD
PRIMARY EXAMINER